IN THE CLAIMS

Please amend the claims as follows:

1-11. (Canceled)

12. (New) A semiconductor device for controlling an inverter circuit comprising:

a complementary PWM signal generation unit for generating a first PWM signal and a second PWM signal corresponding to an inverted signal of the first PWM signal;

a dead time calculating unit for calculating a first dead time and a second dead time, the first dead time determined in response to a comparison between a count value of a timer and a first value stored in a register and the second dead time determined in response to a comparison between a count value of a timer and a second value stored in a register;

a first dead time addition unit for delaying a first edge of the first PWM signal by a first delay value corresponding to the first dead time and for outputting a modified first PWM signal having the first delayed edge instead of the first edge to control the inverter circuit; and

a second dead time addition unit for delaying a second edge of the second PWM signal by a second delay value corresponding to the second dead time, the second edge of the second PWM signal having the same direction of change as that of the first edge of the first PWM signal, and for outputting a modified second PWM signal having the delayed second edge instead of the second edge to control the inverter circuit.

13. (New) The semiconductor device of Claim 12,

wherein the dead time calculating unit includes:

a first register for receiving the first value and the second value from a second register and storing the first value or the second value in response to the receipt; and

a dead time timer for updating a count value and for calculating the first dead time and the second dead time in response to the count value, the dead time timer starting counting in response to either receiving the first edge of the first PWM signal or receiving the second edge of the second PWM signal and stopping counting in response to either a coincidence between the count value of the dead time timer and the first value stored in the first register or a coincidence between the count value of the dead time timer and the second value stored in the first register,

wherein the first value is stored in the first register when calculating the first dead time and the second value is stored in the first register when calculating the second dead time.

14. (New) The semiconductor device of Claim 13,

wherein the complementary PWM signal generation unit includes:

a duty register for storing a third value;

a cycle register for storing a fourth value; and

a cycle timer for updating a count value,

and the first and second PWM signals are generated from a reference PWM signal generated in response to both a coincidence between the count value of the cycle timer and the third value stored in the duty register and a coincidence between the count value of the cycle timer and the fourth value stored in the cycle register,

wherein the second value stored in the second register is transferred to the first register in response to the coincidence between the count value of the cycle timer and the third value stored in the duty register and the first value stored in the second register is transferred to the first register in response to the coincidence between the count value of the cycle timer and the fourth value stored in the cycle register.

15. (New) The semiconductor device of Claim 12,

wherein the dead time calculating unit includes:

a first register for receiving the first value from a first buffer register and storing the first value;

a second register for receiving the second value from a second buffer register and storing the second value; and

a dead time timer for updating a count value and for calculating the first dead time and the second dead time in response to the count value, the dead time timer starting counting in response to either receiving the first edge of the first PWM signal or receiving the second edge of the second PWM signal and stopping counting in response to either a coincidence between the count value of the dead time timer and the first value stored in the first register or a coincidence between the count value of the dead time timer and the second value stored in the second register.

16. (New) The semiconductor device of Claim 15,

wherein the complementary PWM signal generation unit includes:

a duty register for storing a third value;

a cycle register for storing a fourth value; and

a cycle timer for updating a count value,

and the first and second PWM signals are generated from a reference PWM signal generated in response to both a coincidence between the count value of the cycle timer and the third value stored in the duty register and a coincidence between the count value of the cycle timer and the fourth value stored in the cycle register,

wherein the first value stored in the first buffer register is transferred to the first register in response to the coincidence between the count value of the cycle timer and the fourth value stored in the cycle register and the second value stored in the second buffer register is transferred to the second register in response to the coincidence between the count value of the cycle timer and the fourth value stored in the cycle register.

17. (New) The semiconductor device of Claim 12,

wherein the dead time calculating unit includes:

a first register for receiving the first value from a first buffer register and storing the first value;

a second register for receiving the second value from a second buffer register and storing the second value;

a first dead time timer for updating a count value and for calculating the first dead time in response to the count value of the first dead time timer, the first dead time timer starting counting in response to receiving the first edge of the first PWM signal and stopping counting in response to a coincidence between the count value of the first dead time timer and the first value stored in the first register; and

a second dead time timer for updating a count value and for calculating the second dead time in response to the count value of the second dead time timer, the second dead time timer starting counting in response to receiving the second edge of the second PWM signal and stopping counting in response to a coincidence between the count value of the second dead time timer and the second value stored in the second register.

18. (New) The semiconductor device of Claim 17,

wherein the complementary PWM signal generation unit includes:

a duty register for storing a third value;

a cycle register for storing a fourth value; and

a cycle timer for updating a count value,

and the first and second PWM signals are generated from a reference PWM signal generated in response to both a coincidence between the count value of the cycle timer and the third value stored in the duty register and a coincidence between the count value of the cycle timer and the fourth value stored in the cycle register,

wherein the first value stored in the first buffer register is transferred to the first register in response to the coincidence between the count value of the cycle timer and the fourth value stored in the cycle register and the second value stored in the second buffer register is transferred to the second register in response to the coincidence between the count value of the cycle timer and the fourth value stored in the cycle register.

19. (New) The semiconductor device of Claim 12,

wherein the complementary PWM signal generation unit includes:

a duty register for storing a third value;

a cycle register for storing a fourth value; and

a cycle timer for updating a count value,

and the first and second PWM signals are generated from a reference PWM signal generated in response to both a coincidence between the count value of the cycle timer and the third value stored in the duty register and a coincidence between the count value of the cycle timer and the fourth value stored in the cycle register,

wherein said dead time addition unit includes:

a first register for receiving the first value from a first buffer register and storing the first value;

a second register for receiving the second value from a second buffer register and storing the second value; and

a comparator for comparing the count value of the cycle timer with either the first value stored in the first register or the second value stored in the second register and calculating the first dead time and the second dead time in response to a result of the comparison of the comparator.

20. (New) The semiconductor device of Claim 19,

wherein the first value stored in the first buffer register is transferred to the first register in response to the coincidence between the count value of the cycle timer and the fourth value stored in the cycle register and the second value stored in the second buffer register is transferred to the second register in response to the coincidence between the count value of the cycle timer and the fourth value stored in the cycle register.

21. (New) The semiconductor device of Claim 12,

wherein the complementary PWM signal generation unit includes:

a duty register for storing a third value;

a cycle register for storing a fourth value; and

a cycle timer for updating a count value,

and the first and second PWM signals are generated from a reference PWM signal generated in response to both a coincidence between the count value of the cycle timer and the third value stored in the duty register and a coincidence between the count value of the cycle timer and the fourth value stored in the cycle register,

wherein said dead time addition unit includes:

a first register for receiving the first value from a first buffer register and storing the first value;

a second register for receiving the second value from a second buffer register and storing the second value;

a first comparator for comparing the count value of the cycle timer with the first value stored in the first register and calculating the first dead time in response to a result of the comparison of the first comparator; and

a second comparator for comparing the count value of the cycle timer with the second value stored in the second register and calculating the second dead time in response to a result of the comparison of the second comparator.

22. (New) The semiconductor device of Claim 21,

wherein the first value stored in the first buffer register is transferred to the first register in response to the coincidence between the count value of the cycle timer and the fourth value stored in the cycle register and the second value stored in the second buffer register is transferred to the second register in response to the coincidence between the count value of the cycle timer and the fourth value stored in the cycle register.